



# Synaptic Labs' Everspin STT-MRAM Bandwidth Reference design

This tutorial describes how to run the Bandwidth Reference Project on Trenz C10LP / Cruvi FPGA board (CR0010).

## Table of Contents

Set-Up Requirements.....	3
1.0 Contents of the reference project.....	5
2.0 Demo test Application.....	6
3.0 Program the FPGA Bitstream into the FPGA device.....	7
4.0 Run the nios2-terminal application.....	8

# Set-Up Requirements

## Step 1: Obtain core materials

1. Download and install Quartus Prime Standard/Lite 18.1 on your PC, please ensure that your PC meets the required minimum specification.
2. *Obtain Project From SLL and extract bundle to your preferred working folder.*

It is suggested to shorten folders that are too long. This is due to the path length limitation when the Quartus is running in Windows. Rename any long folders .

Step 2: MAX 10 LP Development Board Cruvi Channels



The Trenz CR0010 board contains a power controller that sets the voltage level on the CRUVI channel. Ensure that the EP53A7HQI power controller signals in the top level verilog project file are set to the voltage level required by the memory devices mounted on the Cruvi channels. Check the schematic for more info.

EP53A7HQI	pwr_ctr_vid	pwr_ctr_vid	pwr_ctr_vid	Cruvi J1 Voltage
	2	1	0	
	GND	GND	GND	3.3V
	VCC	GND	GND	2.5V
	VCC	VCC	VCC	3.3V

```
//-----  
//Power Control  
//# EP53A7HQI power and VID control  
//# VID=000 3.3V  
//# VID=100 2.5V  
//# VID=111 1.8V  
//-----  
assign pwr_ctr_enable = 1'b1;  
assign pwr_ctr_vid0   = 1'b1;  
assign pwr_ctr_vid1   = 1'b1;  
assign pwr_ctr_vid2   = 1'b1;
```

ories:  
ial. The

# 1.0 Contents of the reference project

Everspin EMLX Demo reference design projects includes the following files and directories:

- CR0010\_project\_18V\_J1\_xxx folder contains the Quartus Prime and Qsys project files for the first reference project.
- The CR0010\_project\_18V\_J1\_xxx → precompiled folder contains the Quartus Prime precompiled FPGA bitstream and precompiled .elf file
- The CR0010\_project\_18V\_J1\_xxx → ip folder will contain SLL xSPI-MBMC encrypted IP and Altera's DMA IP.
- The CR0010\_project\_18V\_J1\_xxx → software folder is the workspace folder for Eclipse
- The CR0010\_project\_18V\_J1\_xxx → source folder contains the source code for the FlashTest program as used in this xSPI-MBMC Tutorial 001.

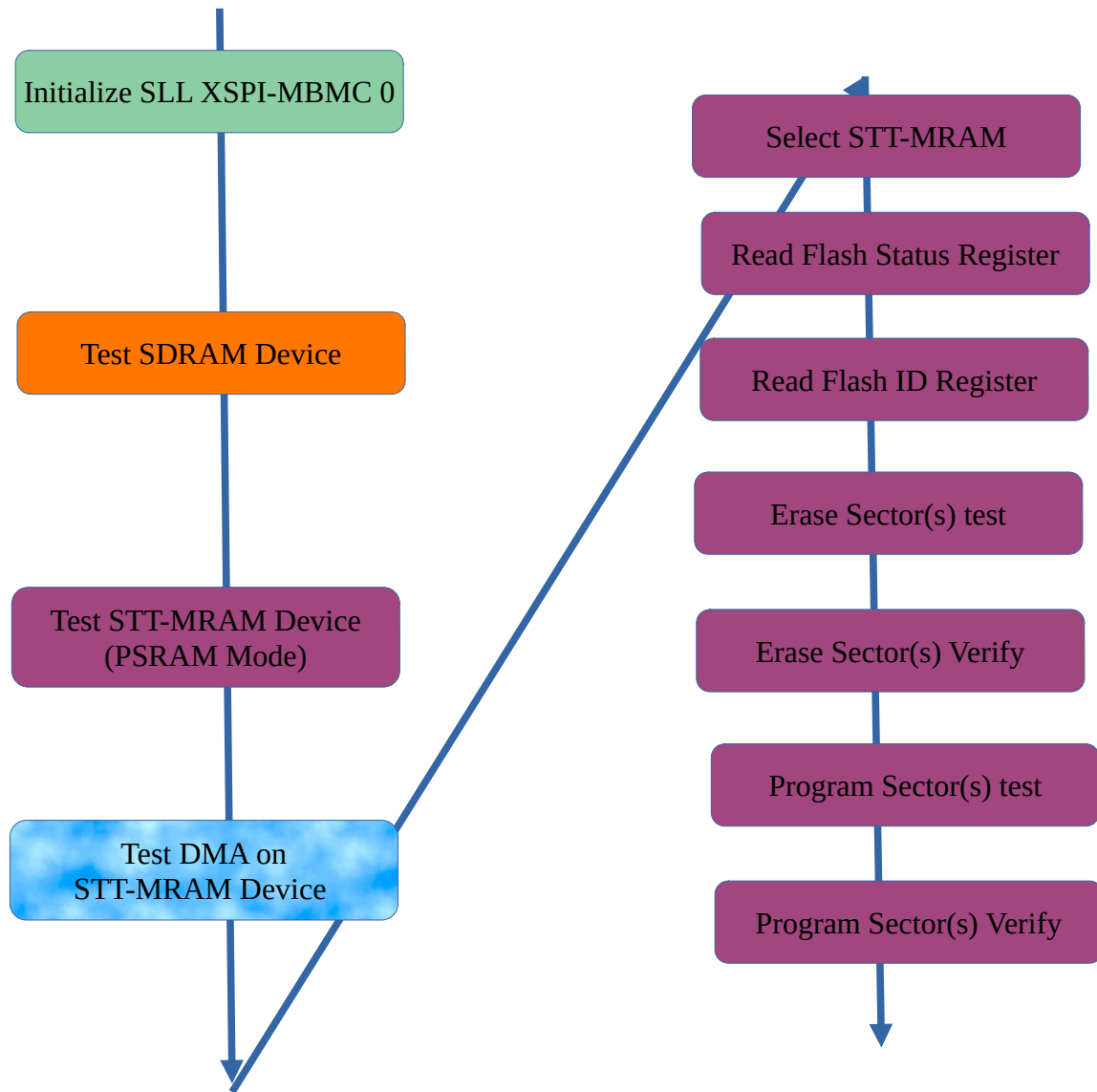
## 2.0 Demo test Application

The pre-compiled project has the following setup

- NiosII running at 100 Mhz
- SDRAM (8 Mbyte) running at 100 Mhz
- Everspin EM064LX (on J1) memory running at 150 Mhz

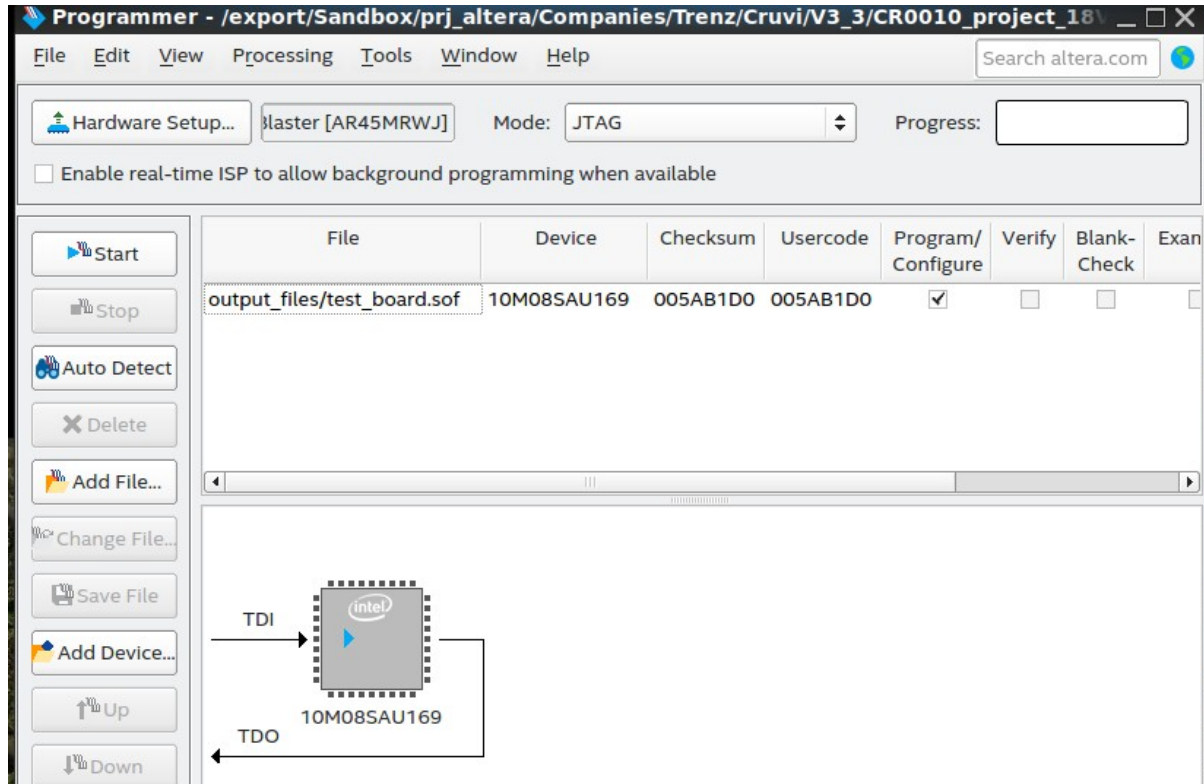
The Flash/SDRAM test application provided with this bundle performs a number of functions to test the SDRAM memory and Flash memory devices.

If errors are encountered, the subsequent tests are bypassed.



### 3.0 Program the FPGA Bitstream into the FPGA device

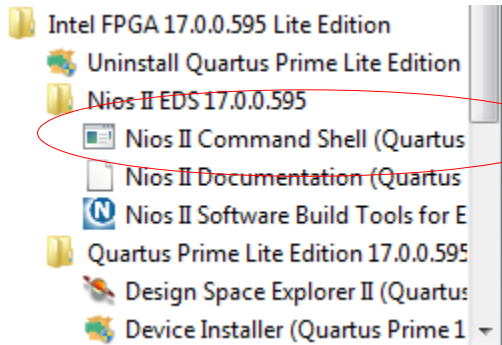
- Connect the Trenz CR0010 C10LP Evaluation kit to the USB port of your computer



- Open the Quartus Prime window
- In the menubar, click on **Tools** then **Programmer** to start the Altera Programmer
- Click on “**Hardware Setup...**”. A new window will open.
- Double Click on the (**Arrow-USB-Blaster [AR45MRWJ]**) device, then click the [ Close ] button.
- Click “**Add File...**” in the programmer window.
  - Go to the **precompiled** folder
  - Double click on **cr0010\_emlx\_test\_board.sof**
- Click the [ Start ] button and the FPGA bitstream will be programmed into the SRAM configuration memory of the FPGA device.

## 4.0 Run the nios2-terminal application

- In Linux: Open a Linux command shell / terminal
- In Windows: Run the **Nios II Command Shell** application from the Windows start menu.



- Change directory to **CR0010\_project\_18V\_J1\_xxx/precompiled** folder
- Type the following command from the terminal:
  - **nios2-download -r -g cr0010\_emlx\_test.elf && nios2-terminal**

```
[mbonnici@localhost precompiled]$ nios2-download -r -g cr0010_emlx_test.elf && nios2-terminal
Using cable "Arrow-USB-Blaster [AR45MRW]", device 1, instance 0x00
Resetting and pausing target processor: OK
Initializing CPU cache (if present)
OK
Downloaded 101KB in 0.2s (505.0KB/s)
Verified OK
```



- Messages similar to the ones below are shown in the console window

```
[mbonnici@localhost precompiled]$ nios2-download -r -g cr0010_emlx_test.elf && nios2-terminal
Using cable "Arrow-USB-Blaster [AR45MRWJ]", device 1, instance 0x00
Resetting and pausing target processor: OK
Initializing CPU cache (if present)
OK
Downloaded 101KB in 0.2s (505.0KB/s)
Verified OK
Starting processor at address 0x00800244
nios2-terminal: connected to hardware target using JTAG UART on cable
nios2-terminal: "Arrow-USB-Blaster [AR45MRWJ]", device 1, instance 0
nios2-terminal: (Use the IDE stop button or Ctrl-C to terminate)

SDRAM memory buffer allocated at address 0x900000
Testing SDRAM

.... Nios II Read/write tests
PSRAM Test : Running pass 1 of 1 passes
Test: Sliding single data bit test within 32-bit word at Address: 0x00900000
- PASS

Test: PSRAM 8/16 bit Byte Enable Test at address: 0x00900000
= 4x08-bit Write:
- 32-bit Read [0]: PASS
- 16-bit Read [0]: PASS
- 16-bit Read [1]: PASS
- 08-bit Read [0]: PASS
- 08-bit Read [1]: PASS
- 08-bit Read [2]: PASS
- 08-bit Read [3]: PASS
= 2x16-bit Write:
- 32-bit Read [0]: PASS
- 16-bit Read [0]: PASS
- 16-bit Read [1]: PASS
- 08-bit Read [0]: PASS
- 08-bit Read [1]: PASS
- 08-bit Read [2]: PASS
- 08-bit Read [3]: PASS
= 1x32-bit Write:
- 32-bit Read [0]: PASS
- 16-bit Read [0]: PASS
- 16-bit Read [1]: PASS
- 08-bit Read [0]: PASS
- 08-bit Read [1]: PASS
- 08-bit Read [2]: PASS
- 08-bit Read [3]: PASS

All Byte-Enabled Tests Passed
```

```

Test: Read and Write to each 32-bit word in range 0x00900000 to 0x00A00000
- Writing value of index into each 32-bit word of span using IOWR operations
- Reading value of index from each 32-bit word of span using IORD operations
- PASS verification test
- Writing value of index into each 32-bit word of span using (cacheable) WR operations
- Reading value of index from each 32-bit word of span using (cacheable) RD operations
- PASS verification test
PSRAM Test :Pass Number: 0, Errors: 0
Testing Everspin EM064LX device in PSRAM Mode

.... Nios II Read/write tests
Test: Read and Write to each 32-bit word in range 0x10000000 to 0x10800000
- Writing value of index into each 32-bit word of span using IOWR operations
- Reading value of index from each 32-bit word of span using IORD operations
- PASS verification test
- Writing value of index into each 32-bit word of span using (cacheable) WR operations
- Reading value of index from each 32-bit word of span using (cacheable) RD operations
- PASS verification test
Press any key to continue :

```

Various test runs are included. When asked, please press any key to continue to the next test sequence.

```

.... SGDMA Test on EM064LX
Altera's Modular SGDMA memory copy benchmarking with integrity verification.
DATA_SOURCE_BASE: 0x10000000
DATA_DESTINATION_BASE: 0x10400000
MAXIMUM_BUFFER_SIZE: 16384
RANDOM_BUFFER_LENGTH_ENABLE: 0
NUMBER_OF_BUFFERS: 128
NUMBER_OF_TESTS: 10
Test number 01 completed for 128 Kilobytes - Avg memory copy throughput is 114 MBytes/s - Avg Read/Write throughput is ~228 MBytes/s.
Test number 02 completed for 256 Kilobytes - Avg memory copy throughput is 114 MBytes/s - Avg Read/Write throughput is ~228 MBytes/s.
Test number 03 completed for 384 Kilobytes - Avg memory copy throughput is 115 MBytes/s - Avg Read/Write throughput is ~230 MBytes/s.
Test number 04 completed for 512 Kilobytes - Avg memory copy throughput is 115 MBytes/s - Avg Read/Write throughput is ~230 MBytes/s.
Test number 05 completed for 640 Kilobytes - Avg memory copy throughput is 115 MBytes/s - Avg Read/Write throughput is ~230 MBytes/s.
Test number 06 completed for 768 Kilobytes - Avg memory copy throughput is 115 MBytes/s - Avg Read/Write throughput is ~230 MBytes/s.
Test number 07 completed for 896 Kilobytes - Avg memory copy throughput is 115 MBytes/s - Avg Read/Write throughput is ~230 MBytes/s.
Test number 08 completed for 1024 Kilobytes - Avg memory copy throughput is 115 MBytes/s - Avg Read/Write throughput is ~230 MBytes/s.
Test number 09 completed for 1152 Kilobytes - Avg memory copy throughput is 115 MBytes/s - Avg Read/Write throughput is ~230 MBytes/s.
Test number 10 completed for 1280 Kilobytes - Avg memory copy throughput is 115 MBytes/s - Avg Read/Write throughput is ~230 MBytes/s.
Press any key to continue :
.....
Testing Everspin EM064LX device in Flash Mode
.....
Testing xSPI EMLX using custom Low Level Driver (DRVR)
Through control port of memory controller IP
R/W MEM : 0x00900000
FLASH : 0x10000000
Programming offset : 0x 100000
Programming span : 0x 100000
Query Flash...
Status Register : 80808080
Status Register : 80808080
Query Flash DeviceId ...
DeviceId : 1017BB6B
Erase Flash : Sector Size 16 K...
Erase Start
Erase Pass
Flash erase time 52
Erase Verify
Erase Verify Pass
PSRAM fill with data
Program Start
Program Pass

```

At the end of the test, a table of results should be printed out in the NiosII Terminal Console Window.

```
-----  
Nios II and Avalon Ports running at 100 Mhz  
-----  
  
-----  
Test Results : Read    -> Write    DMA Bandwidth  
Device       : EM064LX  EM064LX    230 Mbytes/s  
-----  
  
-----  
Test Results          : Data Size 1024 Kbytes  
                      : EM064LX  
Erase Time (ms)       : 52  
Erase Verify Time (ms) : 140  
Program Time(ms)      : 155  
Program Verify Time(ms) : 370  
-----  
  
All tests have completed.
```